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Respectfully submitted,

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Prioritätsbescheinigung über die Einreichung einer Patentanmeldung

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IPC:	H 01 L 29/78

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 6. März 2001
Deutsches Patent- und Markenamt
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Im Auftrag

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FIELD EFFECT TRANSISTOR WITH REDUCED GATE DELAY AND METHOD OF FABRICATING THE SAME

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FIELD EFFECT TRANSISTOR WITH REDUCED GATE DELAY AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to field effect transistors and integrated circuits and, particularly, to a field effect transistor (FET) having a gate electrode with a reduced gate resistance and a method for fabricating the same.

2. Description of the Related Art

The manufacturing process of integrated circuits (ICs) involves the fabrication of numerous semiconductor devices, such as insulated gate field effect transistors, on a single substrate. In order to provide increased integration density and an improved device performance of the field effect transistors, for instance, with respect to signal processing time and power consumption, feature sizes of the field effect transistors are steadily decreasing. In general, decreasing feature sizes, such as the gate length of the field effect transistor, provide a variety of advantages, for example, high package density and small rise and fall times during switching of the transistors due to the reduced gate length and, hence, the reduced channel length. Reducing the gate length of the FET beyond a certain size, however, may result in disadvantages that act to offset advantages obtained by the reduced channel length, *e.g.*, the resistance of the gate electrode having the reduced gate length increases with decreasing gate length. As a result, a delay of the voltage applied to the gate electrode for controlling the channel can be observed. Especially in modern ultrahigh density circuits, the gate length is trimmed down to 100 nm and less, so that the available gate cross section for transmitting the voltage applied to the gate electrode is not sufficient to insure the high-speed signal transmission

required for obtaining the fast switching times of modern integrated circuits such as microprocessors driven by clock frequencies of 1 gigahertz and more.

To clearly demonstrate the problems involved with steadily decreasing feature sizes of modern ultrahigh density integrated circuits, a typical prior art process flow will be described with reference to figures 1a to 1d, in which the problems involved with the formation of the gate electrode are detailed. As the skilled person will easily appreciate, the figures depicting the typical prior art process flow and the typical prior art device are merely of a schematic nature, and transitions and boundaries illustrated as sharp lines may not be imparted as sharp transitions in a real device. Furthermore, the description of the typical prior art process and device refers to standard manufacturing procedures without specifying typical process parameter values used for these procedures, since individual processing steps may be accordingly adapted to meet specific design requirements. Moreover, only the relevant steps and features of the transistor device are shown in the figures.

In figure 1a, a schematic cross-sectional view of a field effect transistor manufactured in accordance with a typical CMOS processing is illustrated. In figure 1a, a field effect transistor 100 is schematically shown in a manufacturing stage prior to patterning a gate electrode. In a silicon substrate 101, shallow trench-isolations 102 define an active region 106. A gate insulation layer 103 separates a polysilicon layer 104 from the active region 106. On the polysilicon layer 104, a photoresist layer 105 is patterned.

The formation of the structure shown in figure 1a may be accomplished using the following process steps. After defining the active region 106 by forming the shallow trench-isolations 102, the gate insulation layer 103 is thermally grown on the substrate. Thereafter, a polycrystalline silicon (polysilicon) layer 104 is deposited over the gate insulation layer 103. Then, a photoresist layer is deposited on the polysilicon layer 104, and it is patterned by

photolithography using deep ultraviolet exposure light to result in the patterned photoresist layer 105.

Figure 1b shows a schematical cross-sectional view of the field effect transistor 100 of figure 1a in an advanced manufacturing stage. In figure 1b, a gate electrode 107 is formed over the active region 106, and it is separated therefrom by the gate insulation layer 103. The gate electrode 107 has been formed from the polysilicon layer 104 by anisotropic etching using the photoresist layer 105 as a mask. A lateral extension of the gate electrode 107 in a transistor length dimension, indicated by the arrows 108 and 109 and also referred to as the gate length, is determined by the lithography step and by a subsequent etch trim process performed to further reduce the gate length. A gate height, indicated by arrow 110, is determined by the thickness of the polysilicon layer 104. According to this typical prior art processing, the gate length on the top 120 of the gate electrode 107, as indicated by arrow 109, is essentially equal to the gate length at the foot or bottom 141 of the gate electrode 107, represented by arrow 108.

As can be seen from figure 1b, the cross section of the gate electrode 107 is of substantially rectangular shape and the effective cross section available for charge carrier transportation decreases, as the gate length is scaled down. Moreover, the gate voltage for controlling the channel to be formed in the active region 106 is applied by contact portions that are outside of the active region in the transistor width dimension, which is the dimension extending along a line normal to the drawing plane of figure 1b. Accordingly, the effective sheet resistance of the gate electrode depends on the gate length on the top portion 120 of the gate electrode 107, and, more particularly, the gate sheet resistance increases as the gate length decreases.

Figure 1c schematically shows a cross section of the final field effect transistor 100. In the active region 106, drain and source regions 111 are formed and separated in the transistor length dimension by a channel 114. Side wall

spacers 112 are formed on side walls of the gate electrode 107 and extend along the transistor width dimension. At the top surfaces of the drain region, the source region and the gate electrode, portions 113 of materials having a reduced electrical resistance, for example, consisting of cobalt silicide, are formed.

The portion 113 of reduced electrical resistance above the gate electrode 107, is also of substantially rectangular shape and, therefore, exhibits a gate area available for charge carrier transportation, i.e., cross section that is small, particularly when the gate length is trimmed down to dimensions of 100 nm and beyond. Since the thickness of the polysilicon layer 104 and, hence, the height of the gate electrode 107 is limited to about 1,500 A to 2,000 A with respect to stability of the gate electrode, polysilicon delamination and the like, the transistor 100 suffers from higher gate resistance when the gate length is reduced, thereby significantly deteriorating the performance of the transistor.

In view of the above problems, a need exists for a field effect transistor device having a reduced gate resistance, and for a method for fabricating the gate electrode with reduced gate resistance.

SUMMARY OF THE INVENTION

According to one aspect of the present invention, a transistor comprises a substrate, an active region defined in the substrate, a gate insulation layer formed above the active region, and a gate electrode formed above the gate insulation layer. The gate electrode comprises a middle portion located over the active region, wherein the middle portion has a gate length and a gate height. A cross-sectional area in a plane defined by the gate length and the gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height.

As is common practice, the gate length is herein defined as the lateral extension at the bottom of the middle portion of the gate electrode. The middle portion indicates that part of the gate electrode that is located over the channel region for controlling the conductivity of the channel. The gate height is defined as the extension of the gate electrode perpendicular to the surface of active region on which the gate insulation layer is formed. Thus, according to the present invention, the gate electrode comprises a middle portion that may be scaled down to meet the design requirements such that a reduced channel length can be realized, wherein the cross-sectional area is increased compared to a typical prior art device having a substantially rectangular cross-sectional area. As a consequence, the effective gate resistance is decreased and the device performance with respect to, for example signal delay, is significantly improved..

In accordance with a further embodiment of the present invention, a lower part of the middle portion may be formed such that its lateral extension, i.e. its length dimension, along the gate height dimension is substantially uniform, that is the cross-section is substantially rectangular, and the lateral extension substantially coincides with the gate length. Thus, a "step like" transition from the lower part to an upper part of the middle portion of the gate electrode is provided. The lateral extension of the upper part of the gate electrode at this transition is significantly larger than the gate length. This "T-shaped" cross section of the middle portion of the gate electrode provides an increased cross section area and, thus, the effective gate resistance is significantly reduced. Moreover, due to the present invention, the top surface of the gate electrode is also increased and results in a decreased gate sheet resistance of the gate electrode, which also contributes to an improved signal transmission of the gate electrode. Furthermore, due to an increased surface area, a portion of reduced electrical resistance, for example, comprising a metal, is also increased and, hence, the effective electrical resistance of the gate electrode is further decreased, regardless of the gate length.

According to another aspect of the present invention, a method of manufacturing a field effect transistor having an improved signal performance is provided, the method comprising: providing a substrate and forming an active region thereon, forming a gate insulation layer over the active region, depositing a first gate electrode material having a first thickness and patterning a first portion of a gate electrode, wherein the first portion has a height substantially equal to the first thickness. The method further comprises depositing an insulating layer having a thickness determined by the first thickness, planarizing the insulating layer to expose a surface of the first portion, selectively removing material of the planarized insulating layer so as to reduce the thickness of the insulating layer until a predefined adjustment thickness is obtained to partially expose side walls of the first portion, depositing a second gate electrode material layer over the insulating layer and the first portion, and anisotropically etching the second gate electrode material layer to form a gate electrode including the first portion and an extension portion laterally extending beyond the first portion, wherein a cross-sectional shape of the extension portion is determined by the adjustment thickness.

According to the method of the present invention, the gate electrode is formed in two steps, wherein the first step determines the final gate length of the transistor and the second step provides for the extension portion to significantly increase the cross section of the gate electrode. Moreover, the method allows to define a cross-sectional shape of the gate electrode by adjusting the thickness of the insulating layer so that the resulting cross-sectional area of the gate electrode can be reliably and reproducibly obtained, since the deposition and etching processes involved in forming and patterning the insulating layer are well-controllable.

In accordance with further embodiments of the present invention, the process of selectively removing material of the insulating layer comprises using a slow chemical etch solution that is highly selective with respect to the first gate electrode material layer. Alternatively, selectively removing the insulating layer

may comprise forming one or more etch stop layers on the main portion prior to the deposition of the insulating layer. Hence, the method can easily be implemented into a standard process flow so as to guarantee efficiency and cost-effectiveness of the manufacturing process. Moreover, according to the present invention, the gate electrode having an extension portion with increased lateral extension does not require any additional cost intensive photolithography and, hence, does not require any additional aligning steps. This characteristic is also referred to as a "self-aligned" process.

Further advantages and objects of the present invention will become more apparent from the following detailed description and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages and objects of the present invention will be explained in greater detail by the following detailed description when taken with reference to the accompanying drawings in which:

Figure 1a shows a schematical cross section of a typical prior art field effect transistor at an initial manufacturing stage;

Figure 1b shows a schematical cross-sectional view of the device of figure 1a with a substantially rectangular polycrystalline gate electrode;

Figure 1c schematically shows a cross section of the final transistor device;

Figure 2a schematically shows a cross section of a portion of a field effect transistor at an early manufacturing stage in accordance with the present invention;

Figures 2b to 2h show schematic cross-sectional views of the field effect transistor of figure 2a in an advanced manufacturing stage; and

Figures 3a to 3c show schematic cross-sectional views explaining an additional process step for improving control of the thickness of the insulating layer.

DETAILED DESCRIPTION OF THE INVENTION

While the present invention is described with reference to the embodiment as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular embodiment disclosed, but rather the described embodiment merely exemplifies the various aspects of the present invention, the scope of which is defined by the appended claims.

Figure 2a shows a schematic, cross-sectional view of a field effect transistor 200 at an early manufacturing stage in accordance with one embodiment of the present invention. In figure 2a, a gate insulation layer 203 and a first portion 207 of a gate electrode are formed above a substrate 201, which may be a semiconductor substrate such as silicon. As previously mentioned, only the middle portion of the gate electrode that is relevant for controlling a channel is depicted in the Figures. Thereafter, lightly doped drain and source regions 211 are formed. The lightly doped drain and source regions 211 are spaced apart from each other with respect to the transistor length dimension, defined as the horizontal direction in figure 2a, by a channel 214. The first portion 207 of a gate electrode to be formed is located above the channel 214 and it is electrically insulated therefrom by the gate insulation layer 203.

Formation of the structure depicted in figure 2a may be accomplished by depositing and patterning both the gate insulation layer 203 and the layer from which a first portion 207 of a gate electrode will be formed using known photolithography and etching techniques. The first portion 207 is comprised of a first gate electrode material, which is, in one illustrative embodiment, a

polycrystalline silicon (polysilicon) layer of a thickness of 1 μm to 2.5 μm. After formation of the first portion 207, the lightly doped drain and source regions 211 are formed by means of ion implantation and a subsequent rapid thermal annealing cycle.

Figure 2b schematically shows a cross-sectional view of the field effect transistor 200 in an advanced manufacturing stage. Figure 2b shows the structure depicted in figure 2a with an insulating layer 220 that is deposited by chemical vapor deposition (CVD) over the first portion 207 and the lightly doped drain and source regions 211. In one embodiment, the thickness of the insulating layer 220 is adjusted so as to match approximately the thickness of the first portion 207, although this is not required. In one illustrative example, the thickness of the insulating layer 220 is adjusted to allow the planarization of the structure by means of CMP. Usually the thickness would exceed or at least match the thickness of the first portion 207. The thickness of the insulating layer 220 depends, for example, on the tool set and the slurry used at the subsequent CMP step. An appropriate thickness of the insulating layer for the subsequent CMP process can easily be determined by those skilled in the art.The insulating layer 220 may preferably be comprised of silicon dioxide or silicon nitride, but any other appropriate dielectric material may be employed.

Figure 2c schematically shows a cross section of the field effect transistor 200 in a further advanced manufacturing stage. In figure 2c, the surface of the structure is planarized so as to expose a top surface 221 of the first portion 207. Planarizing of the surface is accomplished by a chemical-mechanical polishing (CMP) step.

Figure 2d schematically shows a cross-sectional view of the field effect transistor 200, wherein the thickness of the insulating layer 220 is decreased. Accordingly, a portion of the side walls 240 of the first portion 207 are exposed to a predefined degree as indicated by arrow 222. Reducing the thickness of

insulating layer 220 may be accomplished by a chemical etch step that exhibits a high selectivity between the material of the insulating material 220 and the first gate electrode material used to form the first portion 207. By "high selectivity" it is meant that the etch rate of the insulting layer 220 is significantly higher than the etch rate of the first gate electrode material. The final thickness of the insulating layer 220 and, hence, the height of the unexposed surfaces of the side walls 240 of the first portion 207 defines the cross-sectional shape of a bottom portion 207A of a final gate electrode 242 (see Figure 2f) to be formed. The bottom portion 207A is approximately defined by the dashed lines indicated in Figure 2d. The thickness of the insulating layer 220 may be controlled by, for example, a highly selective very slow chemical etch solution which is well known in the art. Further methods for controlling the final thickness of the insulator layer 220 will be described below with reference to figures 3a to 3c.

Figure 2e schematically shows a cross-sectional view of the field effect transistor 200 in a further advanced manufacturing stage. Further to the structure depicted in figure 2d, a layer of a second gate electrode material 204, such as polycrystalline silicon, is deposited over the first portion 207 and the insulating layer 220.

Figure 2f schematically shows a cross-sectional view of the transistor device 200, which further comprises an extension portion 223 formed on the exposed surfaces of the side walls 240 of the first portion 207 so that a complete gate electrode 242 is obtained, wherein only the middle portion of the gate electrode 242 is shown without depicting the part of the gate electrode that is formed outside of the active region. The gate electrode 242 has an upper portion 207B having a lateral extension, indicated by arrow 224, that is larger than a lateral extension of the bottom portion 207A and the foot portion 241 of the gate electrode which approximately defines the gate length of the transistor device 200. The extension portions 223 are formed by an

anisotropic etch step of the second gate electrode material 204, such as a reactive ion etching step known from standard side wall spacer processing.

As can be seen from figure 2f, according to this embodiment, the bottom portion 207A of the gate electrode 242 has a substantially uniform lateral extension, i.e., a substantial uniform gate length, up to a height defined by the thickness of the insulating layer 220. Due to the extension portions 223, the lateral extension of the upper portion 207B of the completed gate electrode 242 has an average value along the height direction of the completed gate electrode 242 that is greater than the effective gate length of the lateral extension of the foot 241 of the bottom portion 207A. Accordingly, the effective cross section of the completed gate electrode 242 is significantly increased compared to a standard prior art device and, hence, the gate resistance and, therefore, the propagation delay of a gate signal is remarkably reduced. In one illustrative embodiment, the lateral extension 224 of the upper portion 207B of the gate electrode ranges from approximately 400 -2000 Å using current photolithographic technologies and techniques, assuming a gate length of the first portion 207, ranging from 350A to 1000A which is a typical value for advanced 0.1um to 0.18um technologies.Thus, in this illustrative embodiment, the lateral extension 224 of the upper portion 207B of the gate electrode 242 is approximately 5 - 100 percent greater than the lateral extension of the bottom portion 207B of the gate electrode 242.

Figure 2g schematically shows a cross-sectional view of the field effect transistor 200 in a further advanced manufacturing stage. Drain and source regions 210 are formed in the lightly doped drain and source regions 211 adjacent to the gate electrode 242 comprised of the upper portion 207B, including the extension portion 223, and the bottom portion 207A including insulating side wall spacers 220A consisting of the residual insulating layer 220. That is, the side wall spacers 220A are positioned between the extension portions 223 and the substrate 201. In order to obtain the structure shown in

figure 2g, the insulating layer 220 is anisotropically etched and an ion implantation is performed to create the drain and source regions 210.

Figure 2h schematically shows the transistor device 200 in a final manufacturing stage. On the top surface 243 of the gate electrode 242, a layer 213 of reduced electrical resistance is formed. In the present example, in accordance with standard CMOS processing, layer 213 of reduced electrical resistance is a cobalt silicide layer. Due to the increased surface area of the "T-shaped" gate electrode 242, and due to the increased cross-sectional area of the gate electrode, the gate sheet resistance, as well as the effective gate resistance, is significantly reduced compared to a typical prior art gate electrode. A Typical prior art gate electrode using standard cobalt silicide would yield a sheet resistance of 8-9 ohm per square. The "T-shaped gate" leads typical to a reduced sheet resistance of 4-6 Ohm per square, depending on the lateral extension of the gate electrode.
The reduced gate electrode results in a lower gate delay and, hence, in a smaller RC constant of the gate electrode which allows a higher operation speed of the transistor device.

Moreover, it should be noted that in the present embodiment, the first gate electrode material, *i.e.*, the first portion 207, and the second gate electrode material are polycrystalline silicon. It is, however, possible to use different materials for the first portion 207 and the extension portions 223. For example, a metal, or a compound of a metal and silicon may be used as the second gate electrode material, *e.g.*, the layer 204. Furthermore, it is possible to perform a silicidation step on the first portion 207 prior to the formation of the extension portions 223. The additional layer of reduced electrical resistance formed in the first portion 207 will further reduce the overall resistance of the gate electrode and, hence, improve signal performance of the FET.

Although the present invention is described with reference to a silicon substrate, a skilled person will readily appreciate that any appropriate substrate can be employed. For instance, the present invention is applicable to an SOI device (silicon-on-insulator) or to any other FET formed on any appropriate semiconductor substrate or insulating substrate.

With reference to figures 3a to 3c, an additional method for improving thickness control of the insulating layer 220 is described.

Figure 3a schematically shows a cross section of the transistor device 200 at the manufacturing stage prior to the deposition of the insulating layer 220. In figure 3a, the side walls 240 and the top surface 221 of the first portion 207, as well as the surface of the substrate are covered by an etch stop layer 230, which may be silicon dioxide that is thermally grown.

Figure 3b shows the device of figure 3a with the insulating layer 220 covering the first portion 207 and the lightly doped drain and source regions 211. By providing the etch stop layer 230, which has a high selectivity to the material of the insulating layer 220 during a subsequent etch step, the final thickness of the insulating layer 220 is precisely adjustable. In the present example, the insulating layer 220 comprises silicon nitride and, hence, silicon nitride can be etched selectively to the polycrystalline silicon material of the first portion 207 and the silicon dioxide of the etch stop layer 230. After the polishing of the insulating layer 220, and the above-described selective etch step, the thermal oxide of the etch stop layer 230 at the exposed side wall portion of the first portion 207 is removed for the subsequent formation of the extension portion 223.

Figure 3c schematically shows a cross-sectional view of the device obtained by performing the process steps as described with reference to figures 3a and 3b. The extension portions 223 are formed on the side walls 240 of the first portion 207 that are not covered by the etch stop layer 230. As in the previously-

described embodiment, the cross-sectional shape of the gate electrode is defined by the final thickness of the insulating layer 220.

It should be noted that other etch stop processes are applicable for defining the final thickness of the insulating layer 220. For example, combinations of different insulating layers may be used as the insulating layer 220 and different etching schemes corresponding to the stack of insulating layers may be employed. Moreover, the etch stop layer 230 may be formed by ion implantation to provide the required etch stop properties on corresponding surface portions of the structure.

Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. Elements and materials may be substituted for those illustrated and described herein.

CLAIMS

1. A transistor, comprising:

a substrate;

an active region defined in said substrate;

a gate insulation layer formed above said active region;

a gate electrode formed above said gate insulation layer, said gate electrode having a middle portion located over the active region, said middle portion having a gate length and a gate height, wherein a cross-sectional area in a plane defined by said gate length and said gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height.

2. The transistor of claim 1, wherein a lower part of said middle portion has a cross-sectional area in the plane defined by the gate length and the gate height that is substantially rectangular.

3. The transistor of claim 2, wherein an extension of an upper part of said middle portion along the gate length direction decreases from bottom to top of said upper part.

4. The transistor of claim 1, wherein the gate length is 100 nm or less.

5. The transistor of claim 1, wherein side walls of the lower part are, at least partially, covered by thermally grown silicon dioxide.

6. The transistor of claim 1, wherein the gate electrode comprises polycrystalline silicon and a metal.

7. The transistor of claim 1, wherein the upper part comprises a metal.

8. The transistor of claim 1, wherein the substrate is a semiconductor substrate.

9. The transistor of claim 1, wherein the substrate is an insulating substrate, and the active region is formed in a semiconductor layer deposited over the insulating substrate.

10. A method of manufacturing a field effect transistor having an improved signal performance, the method comprising:

providing a substrate and defining an active region therein;

forming a gate insulation layer over the active region;

depositing a first gate electrode material layer having a first thickness and patterning a first portion of a gate electrode, the first portion having a height substantially equal to the first thickness;

depositing an insulating layer having a thickness determined by the first thickness;

planarizing the insulating layer to expose a surface of the first portion;

selectively removing material of the planarized insulating layer so as to reduce the thickness of the insulating layer until a predefined adjustment thickness is obtained to partially expose side walls of the first portion;

depositing a second gate electrode material layer over the insulating layer and the first portion; and

anisotropically etching the second gate electrode material layer to form a gate electrode including the first portion and an extension portion laterally extending

beyond the first portion, wherein a cross-sectional shape of the extension portion is determined by the adjustment thickness.

11. The method of claim 10, wherein the first gate electrode material layer and the second gate material layer comprise polycrystalline silicon.

12. The method of claim 11, further comprising depositing a metal layer over the gate electrode and initiate a chemical reaction of the metal layer and the polycrystalline silicon.

13. The method of claim 10, wherein the first thickness is in the range from 1μm to 2.5μm.

14. The method of claim 10, wherein the insulating layer comprises at least one of silicon dioxide and silicon nitride.

15. The method of claim 10, wherein selectively removing material of the insulating layer comprises using a slow chemical etch solution that is highly selective with respect to the first gate electrode material layer.

16. The method of claim 10, wherein selectively removing material of the insulating layer comprises forming one or more etch stop layers on the first portion prior to depositing the insulating layer.

17. The method of claim 16, wherein at least one of the one or more etch stop layers comprises thermally grown silicon dioxide, wherein a thickness of the thermally grown silicon dioxide affects the shape of the extension portion.

18. The method of claim 17, further comprising removing the one or more etch stop layers prior to depositing the second gate electrode material layer.

19. The method of claim 17, wherein the insulating layer comprises silicon nitride.

20. The method of claim 16, wherein at least one of the one or more etch stop layers is formed by ion implantation.

21. The method of claim 10, wherein depositing the second gate electrode material layer comprises depositing two or more layers.

22. The method of claim 21, wherein the two or more gate electrode material layers comprise different materials.

23. The method of claim 22, wherein one of the two or more gate electrode material layers comprises a metal.

24. The method of claim 10, wherein the substrate is a semiconductor substrate.

25. The method of claim 10, wherein the substrate is an insulating substrate and the method further comprises forming a layer of active material over the insulating substrate.

26. The method of claim 10, wherein the extension portion is used as an implantation mask during formation of the drain and source.

ABSTRACT

A transistor formed on a substrate comprises a gate electrode having a lateral extension at the foot of the gate electrode that is less than the average lateral extension of the gate electrode. The increased cross section of the gate electrode compared to the rectangular cross-sectional shape of a prior art device provides for a significantly reduced gate resistance while the effective gate length, i.e., the lateral extension of gate electrode at its foot, may be scaled down to a size of 100 nm and beyond. Moreover, a method for forming the field effect transistor described above is disclosed.

RELEVANT PRIOR ART TO BE CITED

None

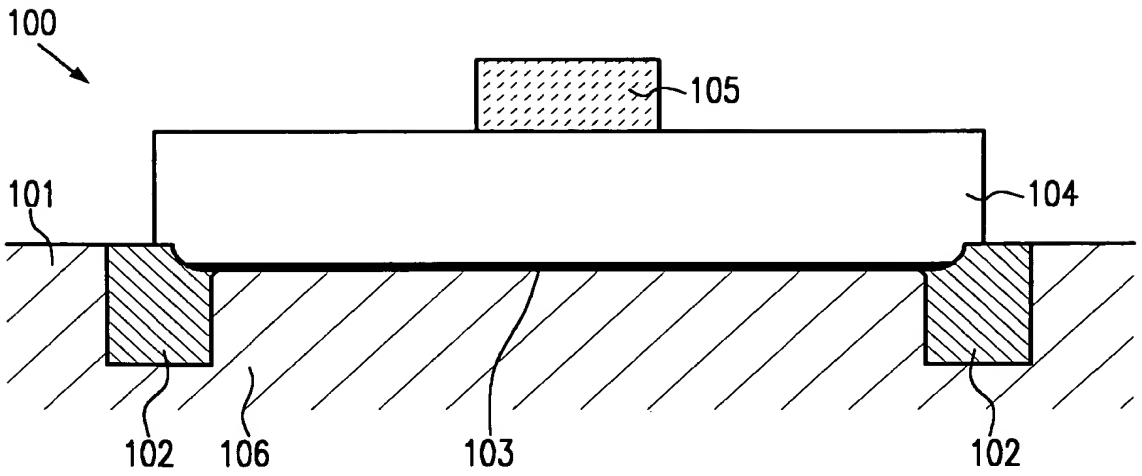

FIG. 1a
(PRIOR ART)

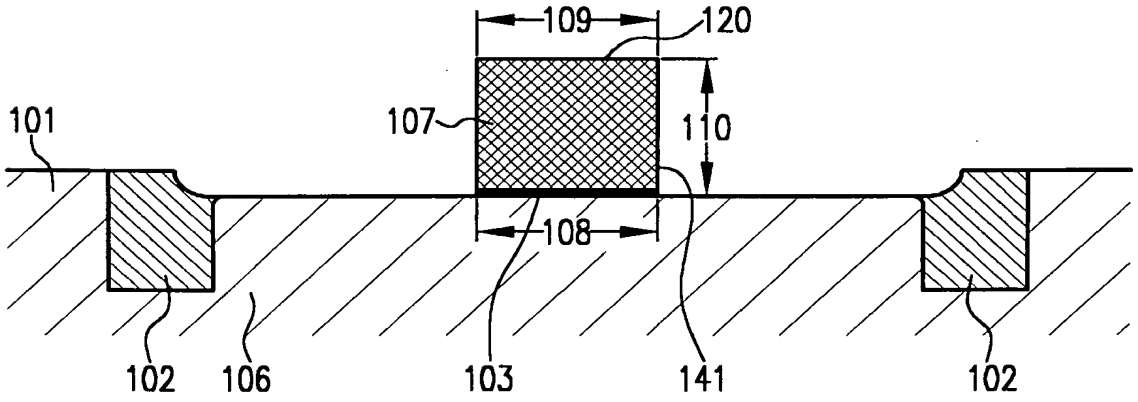

FIG. 1b
(PRIOR ART)

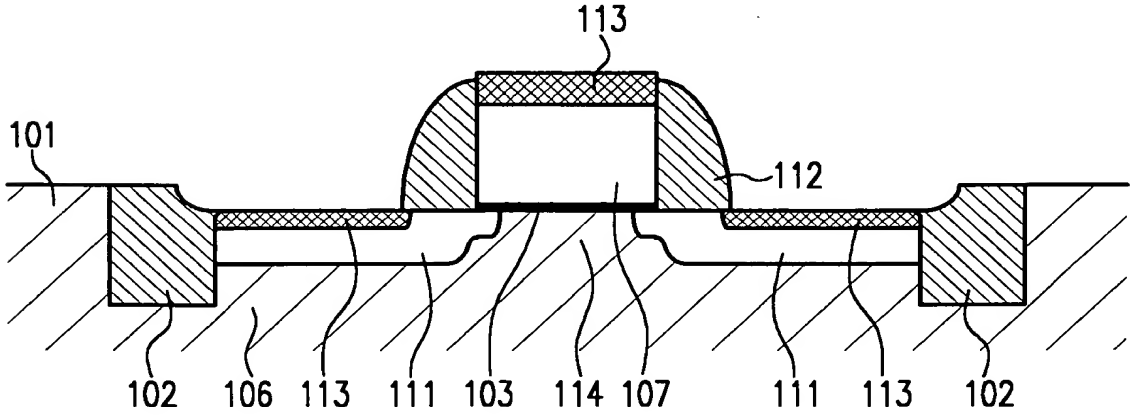

FIG. 1c
(PRIOR ART)

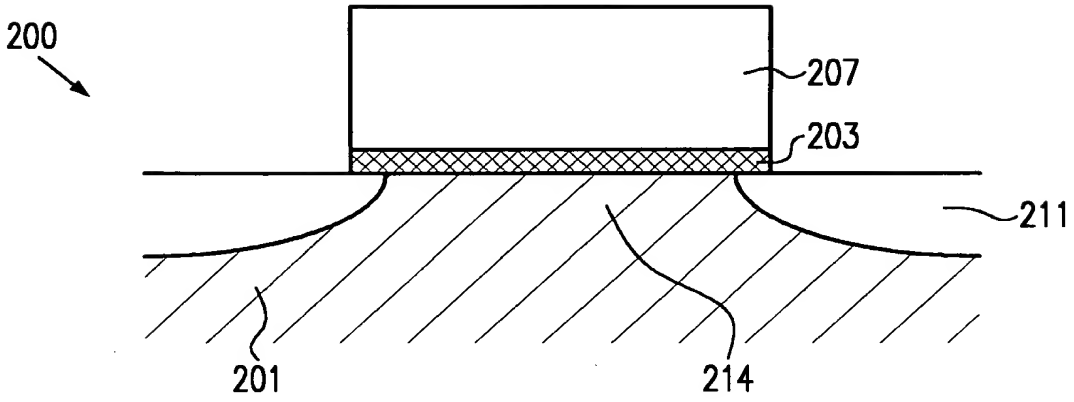

FIG. 2a

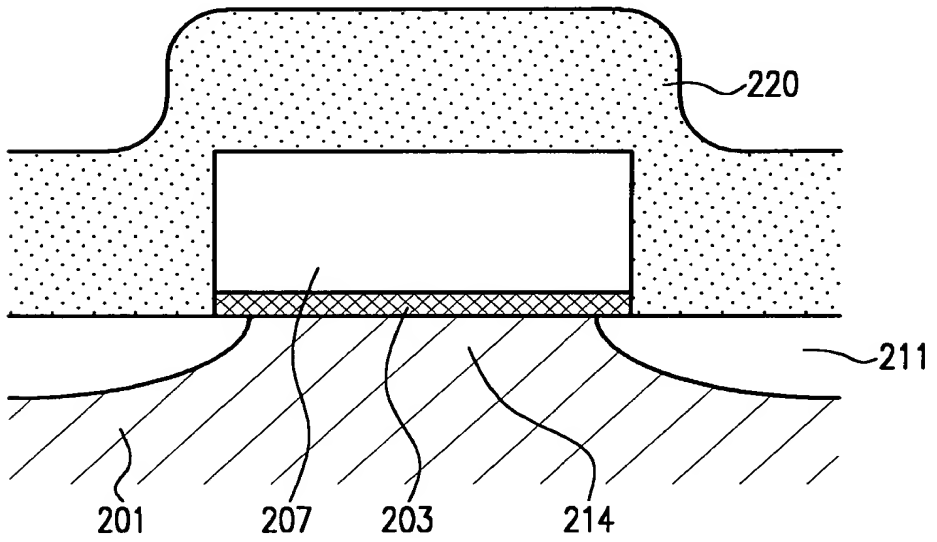

FIG. 2b

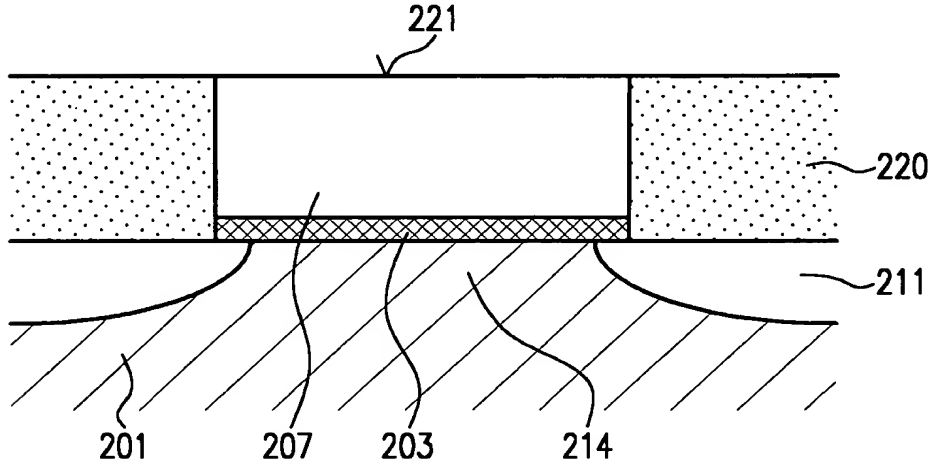

FIG. 2c

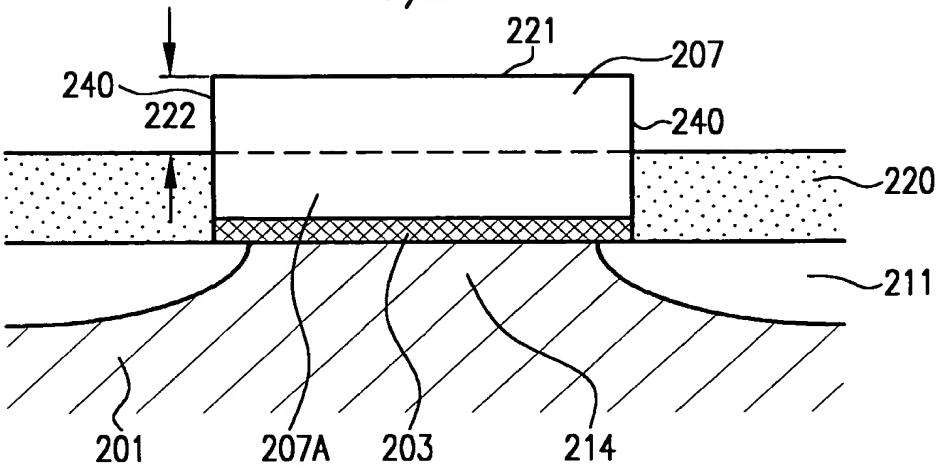

FIG. 2d

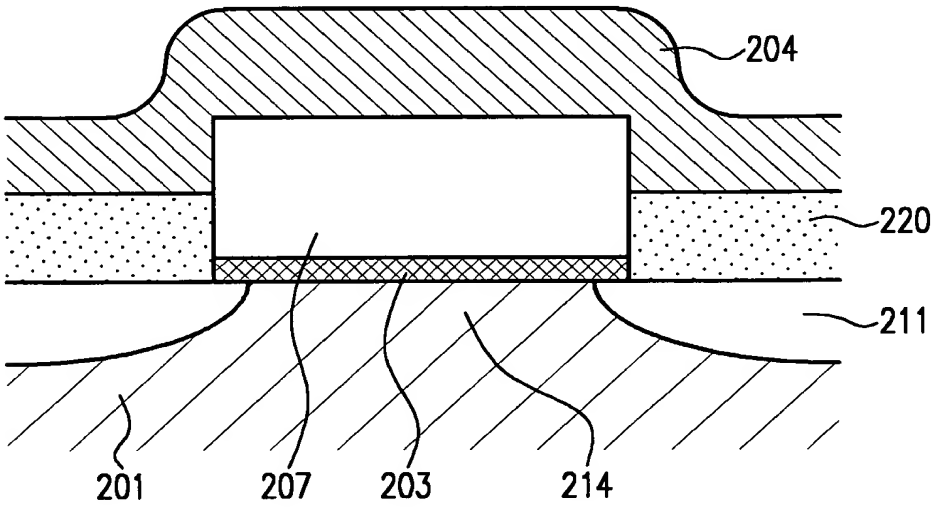

FIG. 2e

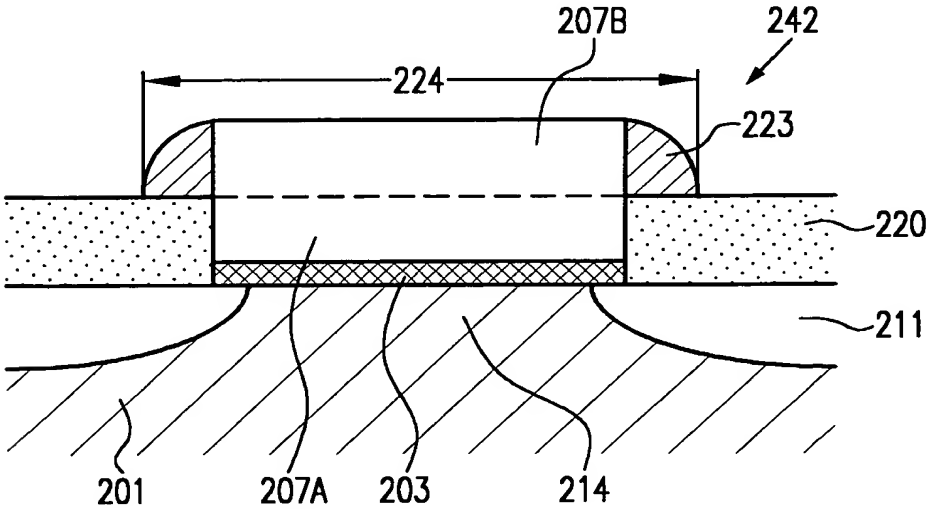

FIG. 2f

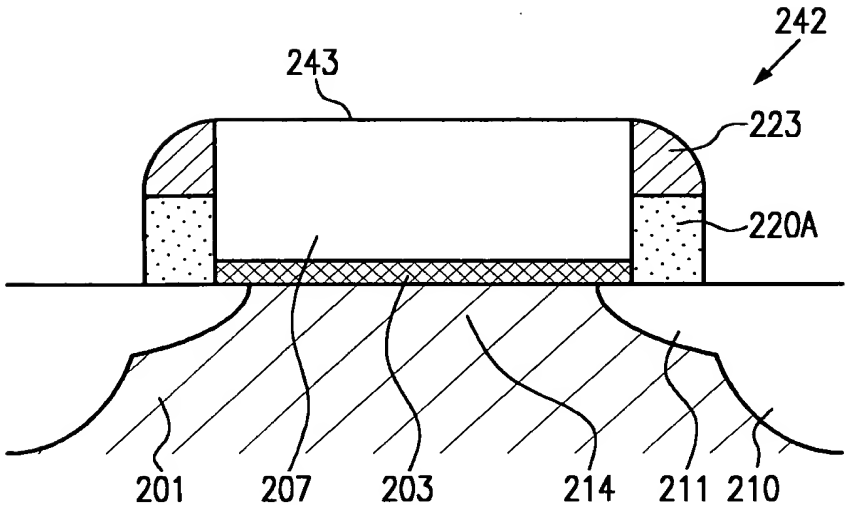
242
243
223
220A
201
207
203
214
211
210

FIG. 2g

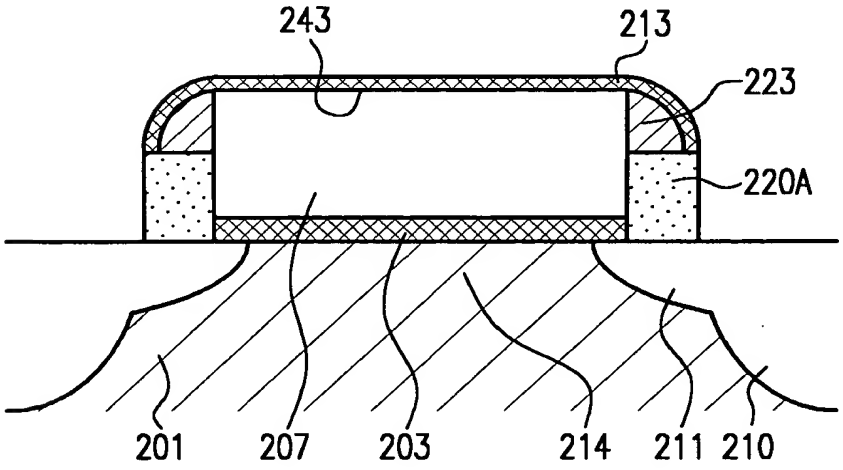
243
213
223
220A
201
207
203
214
211
210

FIG. 2h

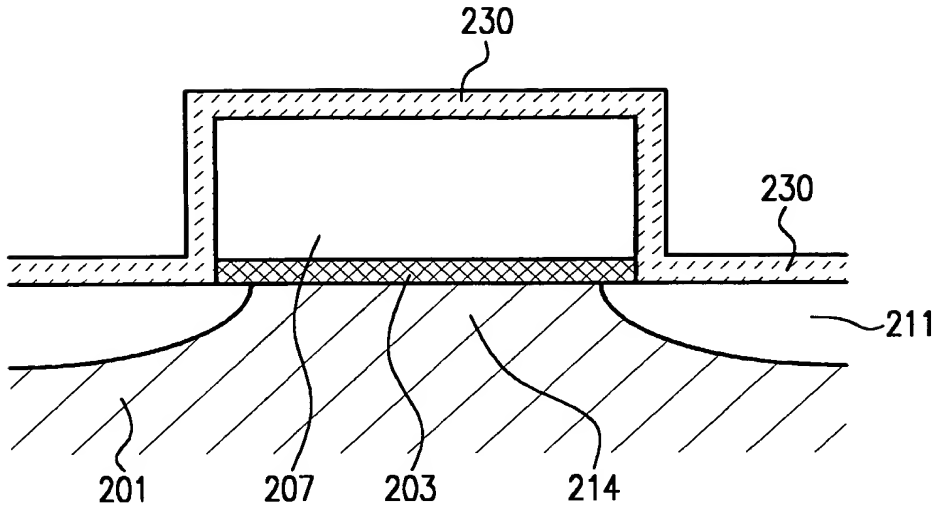

FIG. 3a

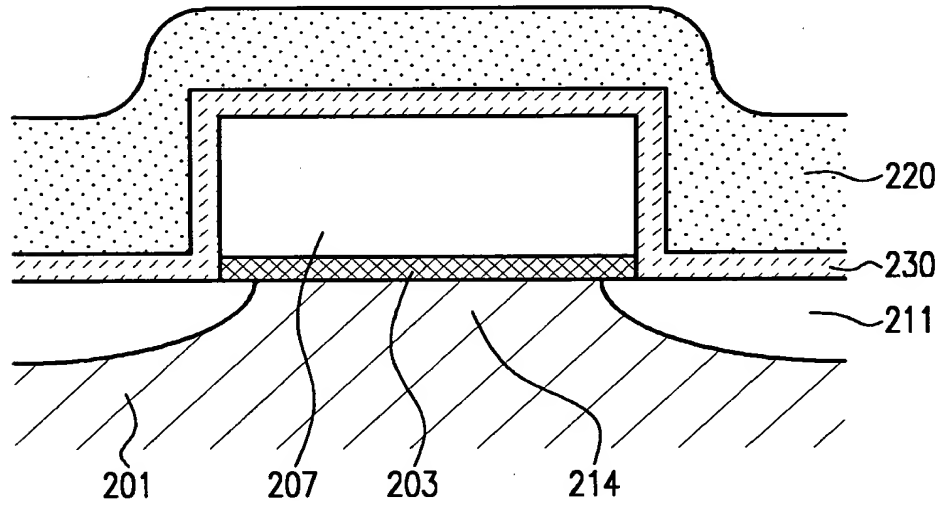

FIG. 3b

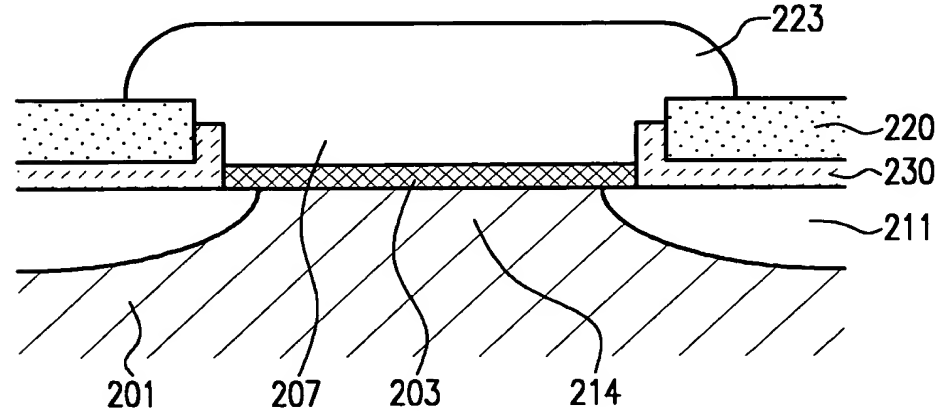

FIG. 3c